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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/853,769	05/14/2001	Takashi Hotta	500.28166CX2	7218

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
11/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/853,769	HOTTA ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-22 and 27-40* is/are pending in the application.

4a) Of the above claim(s) *1-16 and 23-26* is/are withdrawn from consideration.

5)☒ Claim(s) *27-35 and 37-40* is/are allowed.

6)☒ Claim(s) *17-22 and 36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/14/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 17-22,27-40 are presented for examination. Claims 1-16, 23-26 have been canceled.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 17-22,36 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeGroot (4,766,564) in view of Chevillat (4,615,004).

3. As to claims 17, 18, 21,22 ,36, DeGroot taught a system comprising at least :
a) a register for storing data (see fig.1);
b) a plurality of arithmetic operation units to execute plurality of instructions stored in memory in parallel (see fig.1 , ADD, MUL);
c) a plurality of signal lines for sending data stored in the register to an arithmetic unit (see the output connection 22,24 of the register to the input of ADD and MUL in fig.1);
d) a second plurality of signal lines for storing.result data from the arithmetic units in register (see output of ADD and MUL to the input of register in fig.1):
e) a bypass circuit (adder bypass bus and mul bypass bus) for connecting the first and second plurality of signal lines to use data resulting from the arithmetic output for next cycle (see fig.1, see the bypass bus with the switches from the arithmetic units to the instruction, see the control input of the arithmetic units), and the bypass being controlled, by ns of arithmetic instructions in col.3, lines 1-46, see fig.3, see also col.5, lines 17-42 for bypass cycle).

4. DeGroot also included bypass for transferring the data between the different arithmetic units (see the input connection to the switch at each input of the arithmetic units in fig.3, see also limitations already set forth in this action).

5. DeGroot did not specifically showed the fetching of the plurality of instructions at one time as claimed. However, Chevillat disclosed a system for fetching plurality of instructions in parallel (see the instructions fetched in single machine cycle in col.7, lines 32-39). It would have been obvious to one of ordinary skill in the art to use Chevillat in DeGroot for including the fetching of plurality of instructions at one time as clamed because the use of Chevillat could provide DeGroot the capability to schedule the processing of instructions in greater number at a given time, thereby increasing the bandwidth of the instruction processing, and it could be readily achieved by configuring the fetching unit of Chevillat into DeGroot with modified system parameters (such as the instruction width, and instruction number) so that' the fetching of plurality instructions could be recognized by DeGroot at a predetermined fetching cycle, and because DeGroot also taught that a greater number of instructions could be executed in a single cycle for faster operation speed (see co1.1, lines 11-20), which an indication the applicability for fetching more instructions in a given time in order to adapt to faster execution speed, and therefore, it would have been recognizable by one of ordinary skill in the art that the instructions fetched in single machine cycle by Chevilla would have provided a solution for the improvement on DeGroot's single cycle execution to achieve a faster operation speed (see DeGroot 's co1.1, lines 11-20) 17. DeGroot is used as primary reference because it shows the detailed structure of the bypass circuit and the connections of the plurality of switches. Chevillat is used to supplement the teaching of the fetching instructions in parallel.

6. As to claims 19,20, see the switches with the adder bypass bus and mul/bypass bus in fig.3, see also fig.1, see the bypass bus with the switches from the arithmetic units to the input of the arithmetic units.

7. Claims 27-35,37-40 are allowable over the art of record for reciting the combined features of the sequencer, the register for storing data, the plurality of arithmetic units, the first plurality of signals lines, the second plurality of signal lines , the bypass circuit/the switches for transferring data between different arithmetic units when instructions executed by different arithmetic units indicate the same address (27-34), the additional features of the data resulting from operation by the arithmetic unit is not only stored in the register, but also sent to another arithmetic units through the bypass (claim 35), the specific connections of first lines, second lines, third lines , fourth lines, first bypass, ands second bypass (37).

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Kinoshita et al. (4,734,849) is cited for the teaching of the use of plurality of instructions using a plurality of arithmetic units (see fig.3A, see col.7, lines 62-68, col.8, lines 1-18, see co1.5, lines 54-68 for instructions from memory).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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